CLAIMS

What is claimed is:

1. A method comprising:

a) receiving in parallel a plurality of symbol sequences in a first integrated circuit (IC) device, the symbol sequences having been transmitted by a second IC device over a serial point to point link, wherein each symbol sequence includes an instance of a first non-data symbol;

b) buffering the plurality of symbol sequences to compensate for tolerances allowed for a transmit clock of the second IC device and a receive clock of the first IC device; and

c) reducing skew among the plurality of buffered symbol sequences by inserting an instance of a second, different non-data symbol into one but not all of the buffered plurality of symbol sequences immediately preceding an instance of the first non-data symbol.

2. The method of claim 1 wherein in c) the skew is reduced by inserting another instance of the second non-data symbol into another one but not all of the buffered plurality of symbol sequences immediately preceding another instance of the first non-data symbol.

3. The method of claim 1 further comprising after c):

d) detecting an instance of the first non-data symbol in another one but not all of the plurality of symbol sequences,

wherein by c) and d), the non-data symbol has been detected in all of the plurality of symbol sequences so that no further instance of the second non-data symbol is inserted into the buffered plurality of symbol sequences.

4. The method of claim 1 wherein in c), the instance of the first non-data symbol is detected in the buffered plurality of symbol sequences in a cycle of a local clock of the first IC device, and the instance of the second non-data symbol is then inserted in the next cycle of the local clock.

5. The method of claim 1 wherein the first non-data symbol is a PCI Express COM and the second non-data symbol is a PCI Express SKP.

6. The method of claim 3 wherein the plurality of symbol sequences are training sequences.

7. The method of claim 3 further comprising, prior to c), asserting a first deskew enable control signal, and, after c), reducing skew among the plurality of buffered symbol sequences by

asserting a second, different deskew enable control signal; and then

inserting an instance of the second non-data symbol into one of the buffered plurality of symbol sequences immediately following an instance of the first non-data symbol, after detecting the combination of an instance of the first non-data symbol followed by an instance of the second non-data symbol in one but not all of the plurality of symbol sequences.

8. A method comprising:

a) receiving a plurality of symbol sequences in a first integrated circuit (IC) device, the symbol sequences having been transmitted in parallel by a second IC device using the same transmit clock over a serial point to point link that couples the first and second IC devices, wherein each symbol sequence includes an instance of a first non-data symbol;

b) buffering the plurality of symbol sequences and changing the number of times an instance of a second non-data symbol occurs in one of the plurality of symbol sequences; and

c) performing a first deskew process and then a second deskew process,

the first deskew process includes aligning an instance of the first non-data symbol in every one of the buffered plurality of symbol sequences,

the second deskew process includes equalizing the number of instances of the second non-data symbol that follow an instance of the first non-data symbol, in every one of the plurality of symbol sequences.

9. The method of claim 8 wherein the aligning in the first deskew process includes inserting an instance of the second non-data symbol, in a selected one of the buffered plurality of symbol sequences, that leads the instance of the first non-data symbol in the selected sequence.

10. The method of claim 9 wherein the first non-data symbol is a PCI Express COM and the second non-data symbol is a PCI Express SKP.

11. The method of claim 8 wherein the first deskew process is performed during a training session for the link and not during subsequent normal operation of the link, and the second deskew process is repeated for every one of a plurality of instances of a predetermined non-data sequence, that begins with the first non-data symbol followed by the second non-data symbol, during said normal operation.

12. The method of claim 10 wherein the first deskew process aligns the instance of COM that is not part of a PCI Express SKP Ordered Set in the buffered plurality of symbol sequences.

13. An integrated circuit (IC) device comprising:

an elastic buffer having an input to receive a plurality of symbol sequences that were transmitted by another IC device over a serial point to point link, the elastic buffer to provide a plurality of buffered symbol sequences; and

deskew circuitry having an input coupled to an output of the elastic buffer, the deskew circuitry to forward the plurality of buffered symbol sequences with reduced skew in response to an enable control signal being asserted, the deskew circuitry includes

a plurality of deskew buffers,

write pointer logic to load the plurality of buffered symbol sequences into the plurality of deskew buffers,

read pointer logic to provide a plurality of read pointers to unload the plurality of buffered symbol sequences from the plurality of deskew buffers, and

control logic having an output coupled to the read pointer logic, the control logic to, in response to the first instance of a first, predetermined non-data symbol appearing at an output of one of the plurality of deskew buffers since the enable control signal was asserted, a) stall the read pointer for said deskew buffer, and b) generate an instance of a second, different predetermined non-data symbol at an output of the deskew circuitry through which the buffered symbol sequence for said deskew buffer is forwarded.

14. The IC device of claim 13 wherein the read pointer is to be stalled at an entry that contains an instance of the first non-data symbol.

15. The IC device of claim 13 wherein the control logic is to a) release the read pointer and b) stop generating instances of the second predetermined non-data symbol, if an instance of the first predetermined non-data symbol has appeared at an output of every one of the plurality of deskew buffers.

16. The IC device of claim 15 wherein the control logic is to, in response to detecting that a first instance of the first non-data symbol is followed by an instance of the second non-data symbol that are to be loaded into one of the plurality of deskew buffers, a) stall the read pointer for another one of the plurality of deskew buffers after having loaded a second instance of the first non-data symbol that is clock aligned with the first instance, and b) generate an instance of the second non-data symbol at an output of the deskew circuitry through which the buffered symbol sequence for said another deskew buffer is forwarded while preventing said instance of the second non-data symbol, that was detected, from being loaded into said one of the plurality of deskew buffers.

17. The IC device of claim 16 wherein the read pointer is to be stalled for said another deskew buffer at an entry that contains a data symbol.

18. The IC device of claim 13 wherein the first non-data symbol is a PCI Express COM and the second non-data symbol is a PCI Express SKP.

19. A system comprising:

a processor;

a main memory; and

an integrated circuit (IC) device which is communicatively coupled to the processor and the main memory and provides the processor with I/O access, the IC device having link interface circuitry that supports a serial, point to point link, the circuitry includes

an elastic buffer having an input to receive a plurality of symbol sequences that were transmitted by another device over the serial point to

point link, the elastic buffer to provide a plurality of buffered symbol sequences, and

deskew circuitry having an input coupled to an output of the elastic buffer, the deskew circuitry to forward the plurality of buffered symbol sequences with reduced skew in response to an enable control signal being asserted, the deskew logic includes

a plurality of deskew buffers,

write pointer logic to load the plurality of buffered symbol sequences into the plurality of deskew buffers,

read pointer logic to provide a plurality of read pointers to unload the plurality of buffered symbol sequences from the plurality of deskew buffers, and

control logic having an output coupled to the read pointer logic, the control logic to, in response to the first instance of a first, predetermined non-data symbol appearing at an output of one of the plurality of deskew buffers since the enable control signal was asserted, a) stall the read pointer for said deskew buffer, and b) generate an instance of a second, different predetermined non-data symbol at an output of the deskew circuitry through which the buffered symbol sequence for said deskew buffer is forwarded.

20. The system of claim 19 wherein the read pointer is to be stalled at an entry that contains an instance of the first non-data symbol.

21. The system of claim 20 wherein the control logic is to a) release the read pointer and b) stop generating instances of the second predetermined non-data symbol, if an instance of the first predetermined non-data symbol has appeared at an output of every one of the plurality of deskew buffers.

22. The system of claim 19 wherein the control logic is to a) release the read pointer and b) stop generating instances of the second predetermined non-data symbol, if an instance of the first predetermined non-data symbol has appeared at an output of every one of the plurality of deskew buffers.

23. The system of claim 22 wherein the control logic is to, in response to an indication that a predetermined non-data symbol sequence is about to be loaded into one of the plurality of deskew buffers, stall the read pointer for

another one of the plurality of deskew buffers and generate an instance of the second non-data symbol at an output of the deskew logic through which the buffered symbol sequence for said another deskew buffer is forwarded.

24. The system of claim 23 wherein the read pointer is to be stalled for said another deskew buffer an entry that contains a data symbol.

25. The system of claim 19 wherein the first non-data symbol is a PCI Express COM and the second non-data symbol is a PCI Express SKP.

26. The system of claim 19 further comprising a graphics element; and wherein the IC device is a memory controller hub (MCH) that communicatively couples the processor to the main memory and the graphics element.

27. The system of claim 19 wherein the IC device is an I/O controller hub that communicatively couples the processor to peripheral devices.

28. The system of claim 23 wherein the predetermined non-data symbol sequence includes an instance of the first non-data symbol followed by an instance of the second non-data symbol, the instance of the first symbol but not the second symbol being loaded into said one of the plurality of deskew buffers.